Designing with Xilinx Workshop

Esperan

www.esperan.com

Making the most of the Xilinx Virtex technology and Xilinx ISE software.

"Specific Xilinx knowledge, saves a lot of research and provides a concentrated knowledge transfer"

"Good course that emphasises the importance of specifying timing constraints"

"Its far better than reading text books or 'help' text"

"Very informative and useful to designers"

"Pitched at a good level to improve ability to optimise designs"

Train for success...

Overview

Esperan's Designing with Xilinx course combines both technology and methodology content to demonstrate not just the features of Xilinx Virtex technologies and ISE tools, but also how to utilize these features in an HDL-based design flow, using the most popular third-party simulation and synthesis tools. This blend of technology and methodology focus creates an indispensable "value-added" course, far beyond that offered by other training providers, and providing a short-cut to years of Xilinx design experience.

Esperan's effective, focused, training can help engineers create smaller, faster and potentially cheaper designs. For example improving performance by approximately 25% may allow a design to use a device with slower speed grade device and save 50% on the unit cost.

Duration

3 days.

Availability

Regular public workshops are held throughout Europe and North America (check www.esperan.com for schedule). We can also offer standard or customized versions of this workshop, on-site or at the location of your choice.

Objectives

- To provide an in-depth understanding of the Virtex-E and Virtex-II technology resources and the ISE design software features.
- To show you how to write HDL code to target Virtex technology resources and produce optimal synthesis results.
- To demonstrate the tricks and traps of an efficient Xilinx design methodology, utilizing the full capabilities of the Virtex technologies.

Technical Summary

Virtex Technology Family In Depth

A detailed description of the Virtex-E and Virtex-II technology resources, and the advanced features available in the ISE design tools to make the most efficient use of these resources.

"Front to Back" Design Methodology Description

From RTL code to fully implemented design, including use of sophisticated synthesis constraints; Xilinx behavioural and gate level simulation libraries; Core Generator; multi-clock domain timing analysis; floor planning; power estimation and Multipass Place and Route.

Language-Specific Optimisations for Xilinx

HDL coding styles to achieve optimal synthesis results; accessing Virtex device resources with HDL; FSM and data-path optimisation and tracing gate level timing violations back to HDL source code.

Prerequisites

Delegates should have a basic knowledge of digital hardware design and be familiar with their choice of operating system. No prior knowledge of Xilinx tools or technology is assumed. Some previous knowledge of an HDL would be useful, but it is not essential.

Designing with Xilinx Workshop Agenda

Day 1:

- Virtex family architecture and features
  - Configurable Logic Block (CLB)
  - Slice structure
  - SRL16E shift register
  - Memory and multipliers
  - Clock resources
  - Input Output Block (IOB)
- SelectRAM
- Select I/O features in Virtex-E/II
  - Double Data Rate (DDR) registers
  - Digital Controlled Impedance (DCI)
- Low Voltage Differential Signalling (LVDS)
- Virtex routing resources
  - Clock buffers, buses and interconnect
- Floorplan Viewer/ FPGA Editor
- Xilinx design flow overview

Day 2:

- Digital Clock Manager (DCM) features
  - Delay Locked Loop (DLL)
  - Digital Frequency Synthesiser (DFS)
  - Digital Phase Shifter (DPS)
  - Digital Spread Spectrum (DSS)
- Advanced timing analysis in ISE
  - Timing constraints
  - Single clock timing analysis
  - Multi-clock domain timing analysis
- Improving Quality of Results
  - Re-entrant routing
  - Multipass Place and Route (MPRR)
- Xilinx Core Generator
  - Core Generator in a HDL design flow
  - Simulating Core Generator components
- PCB layout considerations
- Configuration
  - Bit-stream encryption

Day 3:

- Review of RTL coding guidelines
- Accessing Virtex device resources from HDL
  - Resets and clock enables
  - Bi-directional I/O
- Issues with resets
- Language specific optimisations
- Architectural optimisations
  - Counters and adders
- Finite State Machine (FSM) optimisations
- Power estimation
- Gate level simulation
  - VITAL libraries
  - SDF annotation
  - Simulation issues

Workshop Labs

The lab exercises demonstrate how the design flow is used in real life design situations. Delegates will experience the entire design flow in detail, through RTL simulation; synthesis; Place and Route; timing analysis and gate level simulation. The labs concentrate on how to use the tools effectively rather than writing HDL source code.

The labs sessions include:-

- Use of Core Generator and Unified Library components: DCM's Double Data Rate I/O's, etc
- Advanced multi-clock domain timing analysis.
- Improving Fmax and device utilization results.
- Using Multi-Pass Place and Route.
- Applying effective synthesis constraints.
- Tracing and fixing timing violations.
- Understanding how to use Xilinx simulation libraries
- Clock domain synchronization.
- Using the floorplan tool.

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